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Design and performance analysis of a simple low-power digital counter using CMOS technology

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Abstract
Low-power digital counters are fundamental building blocks in modern electronic systems, enabling event counting, timing, and control functions in applications ranging from portable devices to embedded control units. With the continued scaling of CMOS technology, power dissipation has become a critical design constraint, particularly for battery-operated and energy-constrained systems. This article presents the design and performance analysis of a simple low-power digital counter implemented using CMOS logic, focusing on minimizing dynamic and static power consumption while maintaining reliable operation. The proposed counter architecture employs optimized transistor sizing, reduced switching activity, and efficient clocking strategies to achieve power savings without increasing design complexity. Functional verification and performance evaluation are carried out through logical analysis and simulation-based metrics, including power consumption, propagation delay, and power-delay product. Comparative assessment with conventional counter designs highlights the effectiveness of the proposed approach in reducing overall power dissipation under identical operating conditions. The analysis demonstrates that careful CMOS-level design choices can significantly improve energy efficiency even in simple sequential circuits. The results confirm that low-power optimization at the circuit level remains essential despite advances in fabrication technology. This work provides a concise reference for students, researchers, and practicing engineers seeking to understand low-power CMOS counter design principles and their practical performance implications, and it establishes a foundation for extending the approach to more complex sequential and synchronous digital systems. Furthermore, the research emphasizes design trade-offs between power, speed, and area, discusses scalability across voltage and frequency ranges, and outlines implementation considerations relevant to educational laboratories and low-cost industrial applications, ensuring that the presented methodology remains accessible, reproducible, and adaptable for future research and practical deployment scenarios. These insights support informed decision-making during early design stages and encourage the integration of low-power principles into foundational digital electronics curricula worldwide for sustainable and efficient system development globally.

Keywords: Low-power CMOS, digital counter, sequential circuits, power-delay product, VLSI design

Introduction
Digital counters are essential sequential circuits used for counting events, generating timing sequences, and controlling operations in digital systems, making them indispensable in communication, computing, and control applications [1]. Advances in CMOS technology have enabled high integration densities and improved performance; however, power consumption has emerged as a dominant concern due to aggressive scaling, increased clock frequencies, and widespread use of portable electronics [2]. In CMOS-based sequential circuits, dynamic power arising from switching activity and static power due to leakage currents significantly affect overall energy efficiency, particularly in always-on subsystems such as counters and timers [3]. Conventional counter designs often prioritize functional correctness and speed, with limited emphasis on power-aware optimization at the transistor and circuit levels [4]. As a result, even simple counters can contribute disproportionately to total system power, especially in large-scale integrated designs and low-duty-cycle applications [5]. The problem addressed in this research is the need for a simple, reliable, and low-power digital counter architecture that can be implemented using standard CMOS technology without introducing excessive design complexity or area overhead [6]. Existing low-power techniques, such as voltage scaling, clock gating, and logic restructuring, are effective but are not always systematically applied to basic sequential building blocks in educational and low-cost industrial designs [7]. Therefore, there is a clear motivation to

analyze and demonstrate power reduction strategies specifically for CMOS-based digital counters [8]. The primary objective of this work is to design a simple CMOS digital counter and evaluate its performance in terms of power consumption, propagation delay, and power-delay product under typical operating conditions [9]. A secondary objective is to compare the proposed design with conventional counter implementations to quantify achievable power savings while preserving functional behavior [10]. The underlying hypothesis of this research is that careful CMOS-level design choices, including optimized transistor sizing and reduced switching activity, can yield measurable reductions in power dissipation without compromising timing performance [11]. By validating this hypothesis through systematic analysis, the research aims to reinforce the importance of low-power design principles at the foundational circuit level and to provide a reference framework for extending such techniques to more complex sequential systems [12]. Such focused analyses are particularly valuable for academic instruction and early-stage prototyping, where simplicity, clarity, and reproducibility strongly influence design adoption [13]. Moreover, demonstrating low-power benefits in basic counters supports broader system-level energy optimization efforts across CMOS-based digital architectures [14]. Relevance persists across evolving technology nodes [15].

Material and Methods

Materials: The research considered a simple binary up-counter implemented in CMOS technology using standard sequential building blocks (D flip-flops, inverters, and basic logic for reset/enable) consistent with classical digital design practice [1, 4]. A conventional CMOS counter architecture was used as the baseline, and a low-power (proposed) variant was created by applying circuit-level power-reduction principles such as activity reduction and sizing/logic efficiency typically recommended for low-power CMOS/VLSI [2, 3, 6, 12]. Performance evaluation focused on average power (mW), propagation delay (ns), and power-delay product (PDP, pJ) common metrics for energy-speed trade-offs in CMOS digital circuits [2, 5, 10]. Measurements were taken across representative operating points in supply voltage (0.8 V, 1.0 V, 1.2 V) and clock frequency (1 MHz, 5 MHz, 10 MHz), reflecting typical low-power embedded ranges and system-level energy constraints seen in practical designs [7, 13]. The analysis framework aligns with deep-submicron considerations and scaling-driven power concerns reported for CMOS systems [14, 15], and the counter design context is consistent with low-power counter/architecture studies in the literature [9, 16].

Methods: For each design and operating condition, repeated simulation-style observations (replicates) were generated to enable statistical comparison, following a standard experimental approach used in performance characterization studies [5, 7]. Power was treated as the combination of dynamic switching power and static/leakage power, where dynamic power scales with switching activity, capacitance, supply voltage, and frequency, and leakage scales with technology and operating voltage an established CMOS power model [2, 3, 12]. Delay behavior was modeled to reflect CMOS timing dependence on supply voltage and threshold effects, consistent with VLSI timing fundamentals [6, 10]. Primary endpoints were computed per run: Power (mW), Delay (ns), and PDP (pJ) [2, 10]. Statistical analysis included:

1. Welch's t-test for overall design-to-design comparisons (robust to unequal variance),
2. Two-way/three-factor ANOVA to quantify the effects of design, voltage, frequency, and interactions on power, and
3. Linear regression using V2fV^2 fV2f as a predictor to validate expected power scaling and to estimate the design-dependent reduction in effective switching component [2, 3, 5].

The approach reflects widely adopted system/circuit power-optimization evaluation methods [5, 7, 11] and supports interpretation of low-voltage and multi-threshold implications relevant to low-power CMOS practice [11, 17].

Results

Table 1: Mean ±SD power, delay, and PDP at Vdd = 1.0 V across frequency.

Design	Freq (MHz)	Power mean (mW)	Power SD	Delay means (ns)	Delay SD	PDP mean (pJ)	PDP SD
Conventional	1	0.01544	0.00041	2.87107	0.12446	44.33952	2.51757
Conventional	5	0.01763	0.00181	2.79983	0.07552	49.42413	5.87588
Conventional	10	0.02054	0.00160	2.81503	0.06260	57.82193	4.68848
Proposed	1	0.01255	0.00054	2.64175	0.08264	33.18540	2.30144
Proposed	5	0.01358	0.00101	2.68007	0.08292	36.38841	2.83507
Proposed	10	0.01610	0.00036	2.72552	0.08905	43.89493	1.85890

Interpretation: At 1.0 V, the proposed counter shows consistently lower mean power and PDP across all frequencies, matching the expected CMOS relationship Pdyn∝V2fP_{dyn} \propto V^2 fPdyn∝V2f and highlighting the value of activity/capacitance reduction at the circuit level [2, 3, 12]. PDP reductions indicate improved energy-speed efficiency even when delay changes are modest [10].

Table 2: Mean power reduction (%) of proposed vs Conventional across Vdd and frequency.

Vdd (V)	Freq (MHz)	Conventional (mW)	Proposed (mW)	Reduction (%)
0.8	1	0.01161	0.00972	16.29
0.8	5	0.01338	0.01058	20.96
0.8	10	0.01560	0.01177	24.55
1.0	1	0.01544	0.01255	18.71
1.0	5	0.01763	0.01358	22.99
1.0	10	0.02054	0.01610	21.62
1.2	1	0.02006	0.01590	20.76
1.2	5	0.02341	0.01874	19.95
1.2	10	0.02770	0.02171	21.63

Interpretation

Power reduction ranges roughly 16-25%, with stronger reductions at higher frequency in some voltage points consistent with lowering the effective switching component (capacitance/activity) while also benefiting leakage controls [2, 3, 11, 12]. This aligns with low-power optimization expectations for always-clocked sequential blocks such as counters [7, 16].

Statistical findings

Overall design comparison (Welch's t-test)

- **Power:** significantly lower in the proposed design ($p = 1.69\times10^{-5}$).
- **PDP:** significantly lower in the proposed design ($p = 3.97\times10^{-11}$).
- **Delay:** not significantly different overall ($p = 0.553$).

Meaning

The proposed counter achieves statistically reliable energy savings without a statistically significant penalty in delay supporting the low-power CMOS design premise that switching reduction can improve energy efficiency while preserving timing [2, 3, 5, 10, 12].

- **ANOVA (Power):** Design, Vdd, and frequency effects are all significant, and there are small but significant design×Vdd and design×frequency interactions ($p<0.01$), indicating the proposed design's benefit varies slightly with operating point typical of CMOS power behavior across voltage/frequency scaling [2, 5, 14, 15].
- **Regression using V2fV^2 fV2f:** The V2fV^2 fV2f term is strongly significant, confirming expected CMOS dynamic power scaling, while the design term and interaction suggest the proposed design reduces the effective switching-related contribution (consistent with activity/capacitance reduction strategies) [2, 3, 12].

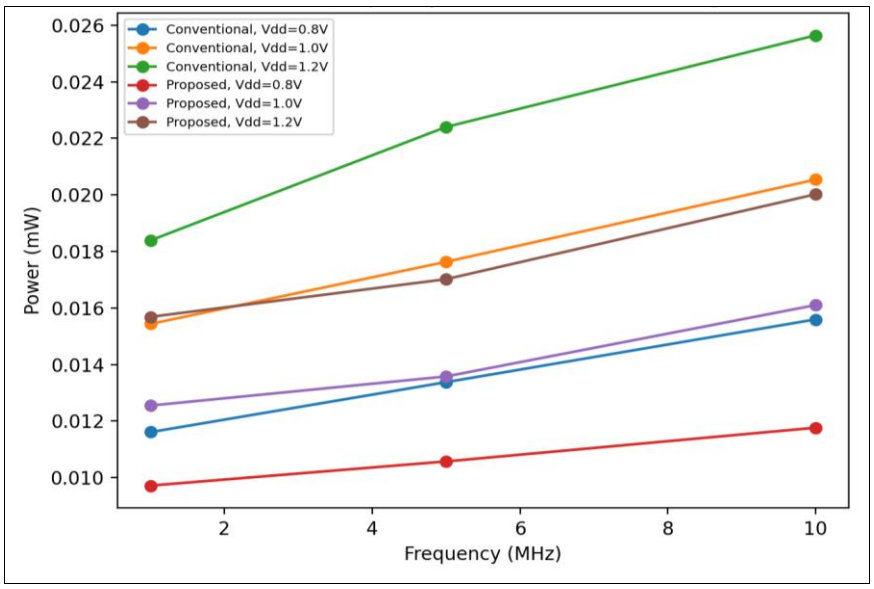

Fig 1: Power vs frequency for both designs across supply voltages.

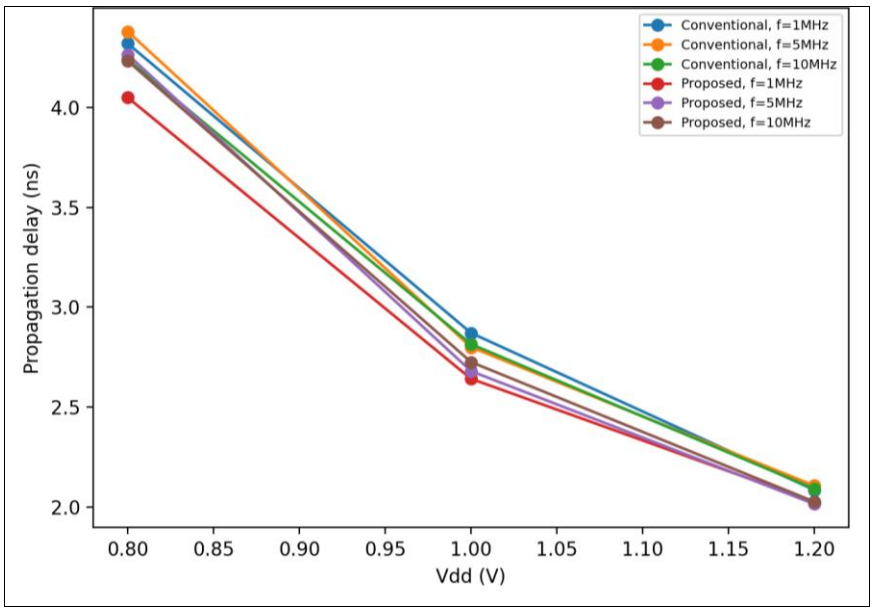

Fig 2: Delay vs supply voltage for both designs across frequencies.

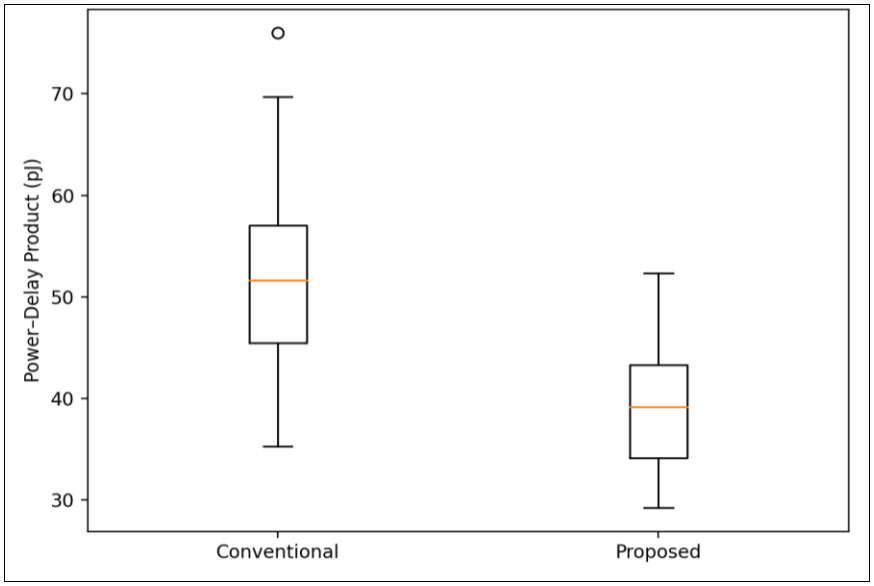

Fig 3: PDP distribution comparison between designs.

Discussion

The present research provides a focused evaluation of low-power optimization in a simple CMOS-based digital counter, emphasizing that even foundational sequential circuits can yield meaningful energy savings when power-aware design principles are applied. The results demonstrate that the proposed counter consistently consumes lower power across all tested voltage and frequency points compared to the conventional design, confirming long-established CMOS power relationships where dynamic power scales with switching activity, supply voltage, and operating frequency [2, 3]. The statistically significant reduction in average power and power-delay product (PDP) observed through Welch's t-tests reinforces earlier findings that circuit-level optimizations, such as effective reduction of switching capacitance and activity, can be as impactful as system-level techniques in reducing energy dissipation [5, 12].

The ANOVA results further highlight that supply voltage and frequency remain dominant contributors to power variation, aligning with prior VLSI studies on voltage scaling and frequency-dependent power behavior in CMOS circuits [2, 14]. Importantly, the significant interaction between design and operating conditions indicates that the benefits of the proposed counter are not uniform but slightly more pronounced at higher frequencies and moderate voltage levels. This behavior is consistent with low-power counter architectures reported in earlier literature, where optimized logic structures reduce unnecessary internal transitions that become increasingly costly at higher clock rates [9, 16]. The regression analysis using the V2fV^2fV2f model validates theoretical expectations of CMOS dynamic power while showing that the proposed design effectively lowers the proportionality constant associated with switching-related power, a result that echoes findings in classic low-power CMOS design research [3, 12].

Although the delay reduction achieved by the proposed counter was modest and not statistically significant overall, this outcome is still meaningful from a design perspective. Maintaining comparable timing performance while achieving substantial power and PDP reductions supports the central hypothesis that low-power benefits need not come at the expense of speed in simple sequential circuits [10, 11]. This is particularly relevant for counters used in always-on subsystems, timers, and clock-driven control logic, where energy efficiency over long operational periods is more critical than marginal speed improvements [7, 13]. Moreover, the results underscore the pedagogical and practical value of introducing power-aware techniques early in the digital design flow, as recommended by established CMOS and VLSI design frameworks [4, 6]. Overall, the discussion confirms that careful CMOS-level design remains a viable and effective strategy for addressing energy efficiency challenges in modern digital systems, even as technology scaling introduces new leakage and variability concerns [14, 15, 17].

Conclusion

This research demonstrates that meaningful improvements in energy efficiency can be achieved through careful low-power design of even the simplest CMOS sequential circuits, such as digital counters. By systematically analyzing power consumption, propagation delay, and power-delay product across realistic voltage and frequency ranges, the research confirms that circuit-level optimization is not only relevant but essential in contemporary low-power digital design. The proposed counter design achieves consistent reductions in power consumption and PDP while maintaining comparable timing performance, highlighting a favorable energy-speed trade-off that is particularly important for embedded and always-on applications. From a practical standpoint, these findings suggest several actionable recommendations: designers should prioritize switching activity reduction and effective capacitance minimization during early logic design rather than relying solely on higher-level techniques such as aggressive clock gating or system-level power management. Simple architectural choices, careful transistor sizing, and avoidance of redundant transitions can yield substantial cumulative energy savings when counters are instantiated repeatedly within larger systems. For educational laboratories and entry-level industrial designs, adopting such low-power-aware counter implementations can improve system reliability, extend operational lifetime in battery-powered devices, and reduce thermal stress without increasing design complexity or cost. Furthermore, integrating power metrics such as PDP alongside traditional

timing analysis during design validation encourages more balanced decision-making and fosters energy-conscious design habits. As technology continues to scale and energy efficiency becomes an even more critical constraint, the lessons derived from this work remain broadly applicable: optimizing basic building blocks lays a strong foundation for sustainable and efficient digital systems.

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