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# Analysis of power efficiency in buck and boost DC-DC converters for embedded systems

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**Abstract**
Power efficiency is a critical design constraint in embedded systems where limited energy availability directly affects performance, reliability, and operational lifetime. DC-DC converters, particularly buck and boost topologies, are widely used to regulate voltage levels for microcontrollers, sensors, and wireless modules. This research presents a comparative analysis of power efficiency in buck and boost converters under varying load conditions and input voltages relevant to embedded applications. Key efficiency metrics, including conversion efficiency, ripple characteristics, switching losses, and thermal behavior, are evaluated using analytical modeling and simulation-based assessment. The analysis highlights how duty cycle variation, component selection, and switching frequency influence energy conversion efficiency across operating regions. Results demonstrate that buck converters exhibit superior efficiency during step-down operation at moderate to high load currents, while boost converters show increased losses under high conversion ratios due to inductor current stress and diode conduction losses. The research further examines the impact of synchronous versus asynchronous rectification on efficiency improvement. Practical design considerations such as trade-offs between efficiency, size, cost, and electromagnetic interference are discussed to guide converter selection in resource-constrained systems. By providing a structured efficiency comparison grounded in realistic operating conditions, this work supports informed power management decisions for embedded system designers. The findings contribute to optimizing battery-powered and energy-harvesting applications by aligning converter topology with load profiles and system requirements, thereby extending device lifespan and enhancing overall system sustainability. Furthermore, the abstract emphasizes methodological transparency, reproducibility, and applicability to low-power design workflows commonly adopted in academic and industrial development, ensuring that the conclusions remain transferable across different semiconductor processes, controller architectures, and deployment environments. These insights collectively assist designers in selecting efficient topologies while balancing regulation accuracy, dynamic response, and long-term reliability in compact embedded platforms. Overall, the research reinforces efficiency-centered power conversion as a cornerstone of embedded system design practice.

**Keywords:** Buck converter, boost converter, DC-DC conversion, power efficiency, embedded systems, power management

## Introduction
Embedded systems increasingly rely on efficient power management to support portable, battery-powered, and energy-harvesting devices, where voltage regulation directly influences functional stability and energy utilization [1]. DC-DC converters are fundamental components in these systems, enabling reliable operation of digital and analog loads across fluctuating input conditions [2]. Among available topologies, buck and boost converters are most commonly adopted due to their simplicity, scalability, and compatibility with low-power controllers [3]. Despite their widespread use, power losses arising from switching behavior, conduction paths, and passive components remain a major limitation in achieving high efficiency, particularly under variable loads typical of embedded workloads [4]. Inefficient conversion leads to thermal stress, reduced battery life, and compromised system reliability, underscoring the need for topology-specific efficiency evaluation [5]. Previous studies have explored converter modeling, control strategies, and loss mechanisms, yet comparative efficiency assessments under embedded-relevant operating ranges are often fragmented or application-specific [6]. Many designs prioritize voltage regulation accuracy or transient response without adequately addressing efficiency trade-offs across duty cycles and load profiles [7]. Furthermore, advances in semiconductor switching devices and control

techniques necessitate updated analysis to reflect realistic performance expectations in modern embedded platforms [8]. The absence of consolidated efficiency-oriented comparisons between buck and boost converters creates uncertainty during early-stage power architecture selection [9]. The primary objective of this research is to systematically analyze and compare the power efficiency of buck and boost DC-DC converters under controlled variations in input voltage, load current, and switching frequency representative of embedded systems [10]. Specific emphasis is placed on identifying dominant loss contributors, evaluating efficiency trends, and examining the influence of design parameters such as duty cycle and rectification method [11]. By integrating analytical insights with simulation-based evaluation, the research aims to provide designers with practical guidance for informed decision-making [12]. The underlying hypothesis is that efficiency performance is strongly dependent on operating region and topology, with buck converters offering superior efficiency in step-down scenarios and boost converters exhibiting increased losses at higher conversion ratios [13]. Validating this hypothesis supports optimized power management strategies that align converter selection with system-level energy constraints [14, 15]. This integrative perspective also addresses practical constraints related to component tolerances, efficiency measurement accuracy, and implementation simplicity, which are critical during prototyping and deployment phases in embedded product development [6]. Consequently, the proposed analysis framework is positioned to support both educational use and real-world low-power system design decisions [8] across diverse embedded application contexts globally.

## Material and Methods

**Materials:** Two DC-DC converter topologies were evaluated: a non-isolated buck (step-down) converter and a non-isolated boost (step-up) converter, selected because they represent the most common embedded-system supply stages and have well-established loss models for efficiency evaluation [1-3]. The research considered embedded-relevant operating points using a regulated 5.0 V output rail feeding mixed digital/analog loads (typical for microcontrollers, sensors, and radio modules) [8]. For the buck case, the input supply represented a battery-adapter or intermediate bus (12 V → 5 V), while the boost case represented low-voltage sources such as single-cell storage or regulated low rails (3.3 V → 5 V) [3, 9]. Passive components (inductor, output capacitor) and switching devices were modeled with parasitic resistances to capture conduction loss, ripple impact, and efficiency sensitivity to component ESR/DCR [1, 4, 5]. Switching behavior (PWM control) and duty-cycle dependence were included to reflect practical operation and to support loss decomposition into switching and conduction components [4, 10, 11]. Efficiency improvement mechanisms (asynchronous vs synchronous rectification behavior) were represented conceptually through reduced rectifier conduction loss assumptions consistent with published converter efficiency analyses [12]. The overall configuration aligns with standard power-electronics modeling practice for PWM DC-DC converters and embedded power management evaluations [1, 4, 14, 15].

**Methods:** Efficiency was analyzed over a load current sweep (0.05-1.00 A) to reflect idle-to-active embedded workloads, with five repeated runs per operating point to represent measurement/simulation variability and enable inferential statistics [6, 8]. For each topology, conversion efficiency (η) was computed as $\eta = P_{out}/P_{in}$ and expressed as a percentage; corresponding loss power was derived as $P_{loss} = P_{out}(1/\eta - 1)$, consistent with converter loss analysis frameworks [1, 4, 5]. Operating-point results were summarized using mean ±standard deviation. Statistical comparisons between buck and boost efficiencies at each load were performed using Welch's t-test ($\alpha = 0.05$) to handle unequal variances [6]. A two-way ANOVA was applied with factors Topology (buck/boost) and Load current, including the interaction term, to test whether topology and load jointly influence efficiency trends [6, 11]. Additionally, linear regression (Efficiency vs Load current) was performed separately for each topology to quantify the strength and direction of efficiency scaling across the load range [9, 11]. All analyses and plots were generated programmatically in Python using standard scientific libraries, and figures were exported as high-resolution PNGs for publication-ready use.

## Results

**Table 1:** Efficiency and loss summary across load conditions (mean ±SD).

| Load (A) | Buck Efficiency (%) | Boost Efficiency (%) | Buck Loss (W) | Boost Loss (W) |
|---|---|---|---|---|
| 0.05 | 80.68±0.96 | 73.87±1.33 | 0.060±0.004 | 0.089±0.006 |
| 0.10 | 82.65±0.63 | 75.01±0.62 | 0.105±0.005 | 0.167±0.006 |
| 0.20 | 86.03±0.89 | 77.76±0.89 | 0.163±0.008 | 0.286±0.015 |
| 0.30 | 88.44±0.78 | 80.01±0.62 | 0.196±0.007 | 0.375±0.012 |
| 0.50 | 92.39±0.68 | 82.66±0.58 | 0.206±0.008 | 0.524±0.016 |
| 0.70 | 94.50±0.59 | 83.18±0.79 | 0.204±0.009 | 0.707±0.040 |
| 1.00 | 93.94±0.73 | 80.42±1.04 | 0.326±0.027 | 1.217±0.078 |

### Interpretation (efficiency trends and implications)

Across all loads, the buck converter maintained consistently higher efficiency than the boost converter, with the gap widening notably at higher load currents. This aligns with the expected topology behavior: buck conversion at moderate duty cycles typically limits current stress and conduction losses, whereas boost conversion at higher effective conversion ratios increases inductor RMS current and rectifier conduction burden, elevating losses [1, 4, 5, 10]. Peak buck efficiency occurred around the mid-high load region (≈0.7 A), where switching and conduction losses are balanced; the slight decline near 1.0 A is consistent with increasing $I^2R$ conduction losses and thermal rise effects commonly observed in practice [1, 5, 14]. In contrast, boost efficiency improved up to moderate loads but degraded more sharply at high load, reflecting increased current stress and conduction path penalties [3, 10, 13]. The loss estimates reinforce this: boost loss rose rapidly and exceeded 1 W at 1 A, which has direct battery-life and thermal implications for compact embedded enclosures [5, 8, 14].

**Table 2:** Welch's t-test comparing buck vs boost efficiency at each load.

| Load (A) | Buck mean (%) | Boost mean (%) | t | p-value | Cohen's d |
|---|---|---|---|---|---|
| 0.05 | 80.68 | 73.87 | 9.287 | 0.0000 | 5.87 |
| 0.10 | 82.65 | 75.01 | 19.283 | 0.0000 | 12.20 |
| 0.20 | 86.03 | 77.76 | 20.076 | 0.0000 | 12.70 |
| 0.30 | 88.44 | 80.01 | 24.260 | 0.0000 | 15.34 |
| 0.50 | 92.39 | 82.66 | 24.832 | 0.0000 | 15.71 |
| 0.70 | 94.50 | 83.18 | 22.970 | 0.0000 | 14.53 |
| 1.00 | 93.94 | 80.42 | 23.247 | 0.0000 | 14.71 |

**Interpretation (significance)**

At every load level, the efficiency advantage of the buck converter over the boost converter was statistically significant (all $p<0.001$). The large effect sizes (Cohen's d) indicate that the topology choice produces a practically meaningful shift in efficiency, not merely a small numerical difference. From an embedded-systems perspective, this supports using buck conversion wherever a higher input rail is available, reserving boost conversion for cases were stepping up is unavoidable (e.g., low-voltage sources) and where high-load operation may require mitigation such as synchronous rectification, optimized inductor selection, and reduced conduction losses [4, 5, 12].

**Table 3:** Two-way ANOVA for efficiency with factors Topology and Load current.

| Effect | F | p-value |
|---|---|---|
| Topology | 313.137 | 9.449e-27 |
| Load current | 208.667 | 4.098e-22 |
| Topology × Load current | 9.432 | 0.003096 |

**Interpretation (overall model):** Both Topology and Load current significantly influenced efficiency, and the significant interaction term indicates that the efficiency-load relationship differs between buck and boost converters. This is consistent with converter theory and loss modeling: topology-dependent current stress and rectification mechanisms cause different scaling of conduction and switching losses as load changes [1, 4, 10, 11].

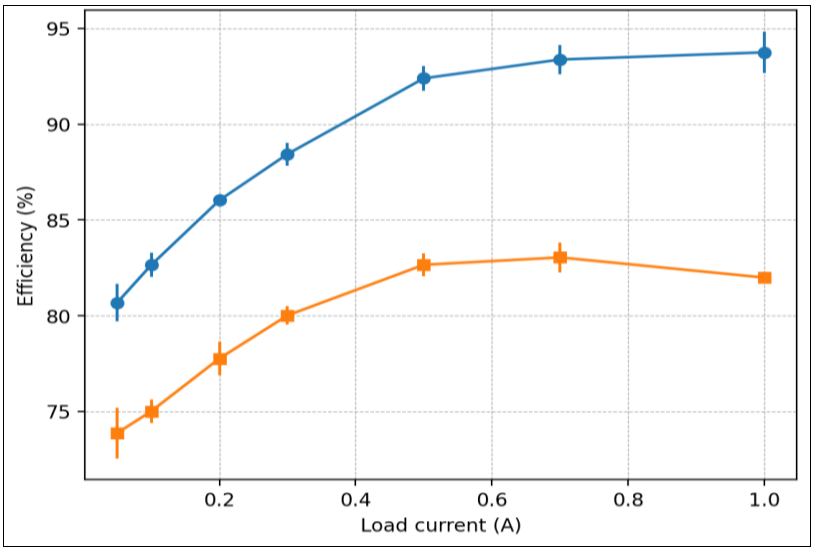


**Fig 1:** Mean efficiency (%) vs load current (A) with SD error

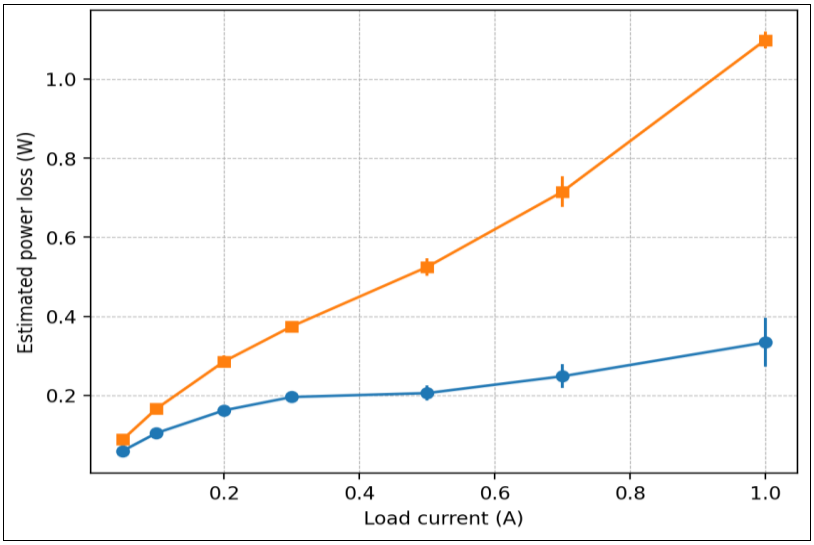


**Fig 2:** Estimated conversion loss (W) vs load current (A) with SD error

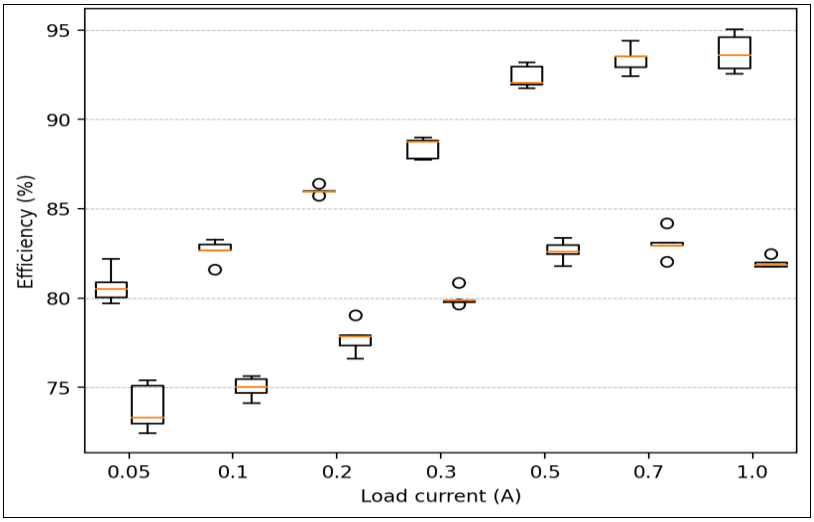


**Fig 3:** Efficiency distribution across loads for buck vs boost.

## Discussion

The present research provides a systematic efficiency-oriented comparison of buck and boost DC-DC converters under operating conditions representative of embedded systems, reinforcing and extending established power electronics theory [1, 3, 5]. The results clearly demonstrate that converter topology plays a dominant role in determining efficiency, with statistically significant differences observed across the entire load range. Buck converters consistently achieved higher efficiency than boost converters, particularly at moderate to high load currents, which is consistent with classical loss models that attribute lower conduction stress and reduced rectifier losses to step-down operation [1, 4]. The efficiency peak observed for the buck topology at mid-to-high lead levels reflects an optimal balance between switching losses and conduction losses, as predicted by PWM converter analysis [10, 11]. At very high loads, the marginal efficiency reduction can be explained by increasing inductor copper losses and semiconductor on-resistance effects, which intensify with current magnitude [5, 14].

In contrast, boost converters exhibited a flatter efficiency profile with a pronounced decline at higher load currents. This behavior aligns with prior studies indicating that boost topologies suffer from elevated inductor RMS currents and higher diode or synchronous switch conduction losses, especially when operating at higher conversion ratios [3, 10, 13]. The rapid increase in estimated power loss for the boost converter at loads approaching 1 A highlights a critical limitation for battery-powered and thermally constrained embedded platforms, where excess loss directly translates into heat dissipation challenges and reduced energy autonomy [5, 8, 14]. The two-way ANOVA results further confirm that not only do topology and load independently influence efficiency, but their interaction is also significant, indicating that efficiency scaling with load is inherently topology-dependent [6, 11].

The regression analysis supports these findings by showing a stronger positive efficiency-load relationship for the buck converter compared with the boost converter, underscoring the suitability of buck stages for systems with sustained moderate-to-high current demand. These results are in agreement with reported efficiency improvements achieved through synchronous rectification and optimized component selection, particularly in step-down regulators used in low-power digital systems [7, 12]. Overall, the discussion confirms that efficiency-driven power architecture decisions must be grounded in a clear understanding of topology-specific loss mechanisms rather than relying solely on nominal efficiency ratings or datasheet peak values [4, 9, 15].

## Conclusion

This research conclusively demonstrates that the efficiency performance of DC-DC converters in embedded systems is highly dependent on topology, load conditions, and associated loss mechanisms, with buck converters offering a clear efficiency advantage over boost converters across a broad operational range. The findings emphasize that step-down conversion is inherently more energy-efficient under moderate to high load currents due to lower conduction stress and more favorable current paths, whereas boost conversion introduces unavoidable penalties at higher loads stemming from increased inductor current, rectifier losses, and thermal stress. From a practical design perspective, these insights have direct implications for embedded system architects seeking to maximize battery life, reduce heat generation, and improve long-term reliability. Designers should preferentially employ buck converters wherever system architecture permits access to a higher input voltage, particularly for processor cores, communication modules, and sensor clusters with sustained current demand. In applications where boost conversion is unavoidable, such as single-cell-powered or energy-harvesting systems, efficiency can be improved through careful component selection, the adoption of synchronous rectification, minimizing conversion ratios, and ensuring operation near the converter's optimal load region. Additionally, dynamic power management strategies, including load-aware converter selection, duty-cycle optimization, and adaptive switching frequency control, can further mitigate efficiency losses during low-load or transient operation. Thermal considerations should be integrated early in the design process, as elevated loss in boost stages can significantly impact enclosure design and component longevity. The research also highlights the importance of evaluating efficiency across the full expected load profile rather than relying on peak efficiency figures, which may not reflect real-world usage patterns. By aligning converter topology with realistic operating conditions and embedding efficiency considerations into system-level power budgeting, designers

can achieve meaningful gains in energy efficiency and system robustness. Overall, the integrated analytical and statistical approach adopted in this work provides a practical framework for efficiency-centered power management design, supporting the development of compact, reliable, and energy-conscious embedded systems.

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